REMARKS

This Amendment is filed in response to the non-final Office Action of June 16, 2004. The due date for response is September 16, 2004. The Applicants thank the Examiner for his careful review of the present application.

Claims 1-20 are pending after entry of the present Amendment.

The Specification is amended to correct typographical errors.

Objection to the Declaration:

The Examiner objected to the Declaration for failing to comply with 37 C.F.R. § 1.67(a), because the Declaration does not state that the persons making the Declaration acknowledge the duty to disclose to the Office all information known to the person to be material to patentability as defined in 37 C.F.R. § 1.56.

In response to the Examiner's objection, a new Declaration has been made to address the deficiency, and it is submitted with this Amendment. Accordingly, the Applicants respectfully request the Examiner to withdraw the objection to the Declaration.

Claim Rejections under 35 U.S.C. § 112, Second Paragraph:

Claims 1-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which the applicants regard as the invention, because of failure to provide sufficient antecedent basis for certain limitations in the claims. The claims have been amended to correct the insufficiently established antecede basis for the affected claim limitations. Accordingly, the Applicants respectfully request the Examiner to withdraw the rejections to the claims.

Rejections under 35 U.S.C. § 102(b):

Claims 1-6 and 8-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Aho et al., "Compilers: Principles, Techniques, and Tools". Applicants respectfully traverse.

One embodiment of the present invention as recited in amended claim 1 is a method of optimizing at least two target machines. The method includes abstracting a rule of instruction scheduling for each of said at least two target machines. A hypothetical machine is generated based on the rule of instruction scheduling for each of said at least two target machines, and the hypothetical machine is targeted.

As described in the specification of the present application, the rule of instruction scheduling for each of at least two target machines are abstracted, for example UltrSPARC II and III. Page 11, line 27-31, page 12, line 1-5, page 12, line 29, line 29-31, and page 13, line 1-2. A hypothetical machine is then generated by incorporating the rule of instruction scheduling for each of the at least two target machines (for example, the characteristics of the UltraSPARC systems having different processors) such that the hypothetical machine will operate satisfactorily on the multiple target machines. Page 13, line 8-11. By targeting the hypothetical machine to address constraints such as latency, register pressure, and blocking versus pipelining of the previous and the current generation machines, a method is provided to optimize at least two target machines. Page 18, line 11-18.

In contrast, Aho et al. provide a general discussion of building compilers. Aho et al. explains that a compiler is a program that reads a program written in one language, the source language, and translates it into an equivalent program in another language, the target language. Page 1, second paragraph. The method described in Aho et al. involves optimizing one target machine, not for at least two target machines. Aho et al. describes creating an intermediate code so that a faster-running machine code will result (page 14, fourth paragraph, Code Optimization). An intermediate code is not a hypothetical machine.

Moreover, the intermediate code is generated from reading instructions from only one machine and used for optimizing one target machine (page 14, fourth paragraph, Code Optimization); whereas, the hypothetical machine recited in claim 1 is generated by using rule of instructions scheduling from at least two target machines and used for optimizing at least two target machines. For at least these reasons, the present invention as recited in amended claim 1 is not anticipated by Aho et al. Therefore, amended independent claim 1 is patentable over Aho et al.

Dependent claims 2-6 drawing their dependencies from independent claim 1 are similarly not anticipated for substantially the same reasons as independent claim 1 and for the additional limitations that each dependent claims respectively recite.

Independent claims 8, 13, and 19 are similarly not anticipated for substantially the same reasons as independent claim 1. Therefore, independent claims 8, 13, and 19 are similarly not anticipated by Aho et al.

Dependent claims 9-12 drawing their dependencies from independent claim 8 are similarly not anticipated for substantially the same reasons as independent claim 8 and for the additional limitations that each dependent claims respectively recite.

Dependent claims 14-18 drawing their dependencies from independent claim 13 are similarly not anticipated for substantially the same reasons as independent claim 13 and for the additional limitations that each dependent claims respectively recite.

Dependent claim 20 drawing it dependency from independent claim 19 is similarly not anticipated for substantially the same reasons as independent claim 19 and for the additional limitations it recites.

Rejections under 35 U.S.C. § 103(a):

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Aho et al., "Compilers: Principles, Techniques, and Tools". The Examiner acknowledges that Aho et al. did not disclose the method of claim 1 wherein said at least two target machines include an UltraSPARC-II configured to operate at a speed of 360 MHz and an UltraSPARC-III configured to operate at a speed of 600 MHz. However, Official Notice is taken that is was known at the time of the invention to make use of UltraSPARC-II and III processors configured at varying MHz ranges within their capabilities. Applicants respectfully traverse.

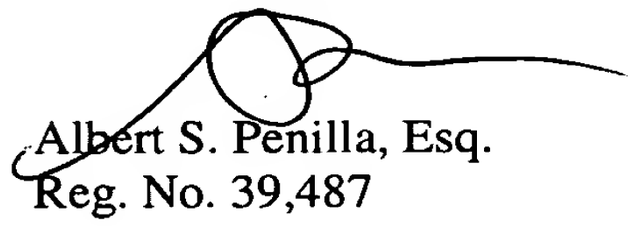
As discussed in the above section, Aho et al. does not disclose generating a hypothetical machine by using the rule of instruction scheduling from multiple target machines. The Examiner takes Official Notice that is was known at the time of the invention to make use of UltraSPARC-II and III processors configured at varying MHz ranges within their capabilities. Applicants respectfully submit that it is impermissible for the Examiner to fill-in the deficiencies in Ah et al. by taking Official Notice and asserting that a person of ordinary skilled would be able to implement features that are completely missing from Aho et al. First, Aho et al. has not disclosed the method of generating a hypothetical machine by using rule of instruction scheduling for each of at least two target machines. Second, Aho et al. has not provided any suggestions or motivations to use UltraSPARC II or III systems as target machines. Unless the Examiner can provide a proper showing from other references to remedy the deficiencies of Aho et al., Applicants respectfully request that the Examiner to withdraw his Official Notice. Since the Examiner has not sufficiently established a prima facie case of obviousness, dependent claim 7 is patentable.

Accordingly, after entry of the present Amendment, the application is now in a condition for allowance. A Notice of Allowance is therefore respectfully requested.

If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any other fees are due in

connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP303). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP



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